**Nepal College of Information Technology**

**Assessment Fall 2013**

Program : BE IT Time : 3 hrs

Semester : Fall (V) FM : 100

Subject : Computer Organization & Architecture PM : 50

* *Candidates are requested to give their answer as far as practicable in their own words.*
* *The figure in the margin indicates the full marks*
* *Attempt ALL question*

1 a) What are the issues while designing an instruction set? Compare an Assembling and Compiling Process 7

b) Design the 8x 2 ROM memory Internal Architecture in

i) Linear Organization

ii) Two Dimensional Organization 8

2 a) Show the hardware to implement the following RTL code for the modulo 6 Counter 7

b) Design a very simple CPU has the following instruction set and Show the RTL code for execute cycle for each Instruction 8

|  |  |  |
| --- | --- | --- |
| Instruction | Instruction Code | Operation |
| SUB | 00AAAAAA | AC🡨AC - M[AAAAAA] |
| AND | 01AAAAAA | AC🡨AC ^ M[AAAAAA] |
| OR | 10AAAAAA | AC🡨AC v M[AAAAAA] |
| INC | 11XXXXXX | AC🡨AC+1 |

3 a) From the above table also design the ALU and Hardwired control unit for the very simple CPU. 7

b) Write a difference between Horizontal and vertical micro code ?What are the guidelines while using vertical microcode design 8

4 a) Describe the microinstruction format? Elaborate a significance of Micro sequencer with diagrams . 8

b) What do you mean by Pipelining ?Explain the conflicts in RISC pipeline how can it resolve . 7

5 a) Write the steps of booth algorithm? Show the trace of the RTL code for Booths Algorithm for X=1110 and Y=1001 8

b) Explain the Hardware implementation of Addition and subtraction algorithm 7

6 a) Define Cache Memory ? How to convert the logical address into to physical address .Explain with diagrams 8

b) When an interrupt occurs? How to implement an I/O port using polling Explain 7

7 Write Short Notes(Any Two) 5X2=10

a) MIMD Architecture

b) VHDL

c) Register Window